Application number 09/881,226
Amendment dated November 22, 2004
Reply to office action mailed May 21, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the applic ition:

Listing of Claims:

Claim 1 (original) A programmable logic integrated circuit comprising:

a programmable logic portion; and

an embedded processor portion coupled to the programmable logic port on and comprising:

a processor; and

a memory block coupled to the processor and comprising:

a memory having a first port and a second port; and

an arbiter coupled to the first port and the second port, wherein i ie arbiter arbitrates access to the memory by the first port and the second port.

Claim 2 (original) The integrated circuit of claim 1 wherein he memory is a dual-port SRAM.

Claim 3 (original) The integrated circuit of claim 2 wherein he programmable logic portion comprises a plurality of logic elements, programmably co ifigurable to implement user-defined combinatorial or registered logic functions.

Claim 4 (original) The integrated circuit of claim 3 wherein he programmable logic portion further comprises a plurality of horizontal and vertical int rconnect lines, programmably coupled to the plurality of logic elements.

Claim 5 (original) The integrated circuit of claim 1 wherein he second port is configurable in width and depth.

Claim 6 (original) The integrated circuit of claim 1 wherein he first port and the second port are both configurable in width and depth.

Application number 09/881,226   PATENT
Amendment dated November 22, 2004
Reply to office action mailed May 21, 2004

Claim 7   (currently amended)   A programmable logic integrated ircuit comprising:

a programmable logic portion comprising a plurality of logic elements, programmably configurable to implement user-defined combinatorial or registered log c functions; and

an embedded processor portion coupled to the programmable logic port on and comprising:

a processor; and

a memory block coupled to the processor and comprising:

a first plurality of memory cells for storing data;

a second plurality of memory cells for storing data;

a first port coupled to the first and second pluralities of r .emory cells;

a second port coupled to the first and second pluralities (f memory cells; and

an arbiter coupled to the first port and the second port,

wherein when the second port is accessing <u>a subset of</u> the first plurality of memory cells, the arbiter prevents the first port from accessing the first plurality of me nory cells, and when the second port is accessing <u>the subset of</u> the first plurality of memory cells, the arbiter allows the first port to access the second plurality of memory cells.

Claim 8   (original)   The integrated circuit of claim 7 wherein he first plurality of memory cells and the second plurality of memory cells are defined by a us r-programmable lock register.

Claim 9   (original)   The integrated circuit of claim 8 wherein he first and second pluralities of memory cells comprise a portion of a dual-port SRAM.

Claim 10   (original)   The integrated circuit of claim 9 wherein he programmable logic portion further comprises a plurality of horizontal and vertical int rconnect lines, programmably coupled to the plurality of logic elements.

Claim 11   (original)   The integrated circuit of claim 10 wherei the second port is configurable in width and depth.

Claim 12   (original)   The integrated circuit of claim 10 wherei the first port and the second port are both configurable in width and depth.

Claims 13-45 (cancelled)

Claim 46   (new)   The integrated circuit of claim 7 wherein vhen the when the second port is accessing a subset of the second plurality of memory cells, the arbiter allows the first port to access the first plurality of memory cells, and when the second ort is accessing the subset of the second plurality of memory cells, the arbiter allows the firs port to access the second plurality of memory cells.

Claim 47   (new)   An integrated circuit comprising:
a programmable logic portion; and
a memory block coupled to the programmable logic portion and compri ing:
        a first plurality of memory cells for storing data;
        a second plurality of memory cells for storing data;
        a first port coupled to the first and second pluralities of memory cells;
        a second port coupled to the first and second pluralities of mem ry cells;
and
        an arbiter coupled to the first port and the second port,
wherein when the first port is accessing a subset of the first plurality of nemory cells, the arbiter prevents the second port from accessing the first plurality of memory ells and allows the second port to access the second plurality of memory cells, and

PATENT

wherein the first plurality of memory cells consists of a number of memory cells and the number is configurable.

Claim 48 (new) The integrated circuit of claim 47 wherein when the first port is accessing a subset of the second plurality of memory cells, the arbiter allows the second port to access the first plurality of memory cells and the second plurality of memory cells.

Claim 49 (new) The integrated circuit of claim 48 wherein the programmable logic portion comprises a plurality of logic elements, programmably configurable to implement user-defined combinatorial or registered logic functions.

Claim 50 (new) The integrated circuit of claim 49 further comprising:

an embedded processor portion coupled to the programmable logic portion and comprising:

a processor; and

the memory block.

Claim 51 (new) The integrated circuit of claim 49 wherein the number of memory cells in the first plurality of memory cells is configurable by programming a register.

Claim 52 (new) The integrated circuit of claim 49 wherein the first port and the second port are configurable in width and depth.

Claim 53 (new) The integrated circuit of claim 49 wherein the integrated circuit is a programmable logic device.